Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit for monitoring protocol-defined information packets including both data and packet routing information, wherein the protocol-defined information packets are either response packets or request packets and are put onto an interconnect by one or more modules for analysis including debugging of the circuit, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, said circuit comprising:

circuitry for determining [[if]]whether [[the]] information in a protocol-defined information packet matches one or more conditions and wherein the determining circuitry identifies the source and type of the matched protocol-defined information packet; [[and]]

circuitry responsive to determining that the information in the protocol-defined information packet matches one or more conditions for capturing a portion of the matched protocol-defined information packet

circuitry for preventing ~~a module~~ the source of the matched protocol-defined information packet from putting further protocol-defined information packets onto said interconnect ~~if it is determined that information on the interconnect matches said one or more conditions~~; and

transferring the portion of the matched protocol-defined information packet to a debug module for analysis.

2. (Cancelled)

3. (currently amended) A circuit as claimed in claim 1, wherein said ~~information comprises requests and responses~~ circuit is a split-transaction bus capable of carrying a plurality of protocol-defined information packets simultaneously.

4. (currently amended) A circuit as claimed in claim 1, wherein said circuitry for capturing the portion of the matched protocol-defined information packet includes at least two independent buffers ~~preventing a module from putting further information onto the interconnect comprises a register~~.

5. (Currently Amended) A circuit as claimed in claim [[4]]1, wherein the circuitry for determining whether information in a protocol-defined information packet matches one or more conditions includes two or more impendent registers ~~register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect~~.

6. (currently amended) A circuit as claimed in claim [[4]]5, wherein a location is defined in said register for each module, the location being independent of the address of the module used by the interconnect.

7. (Currently Amended) A circuit as claimed in claim 1, further comprising allowing additional protocol-defined information packets from the source of the matched protocol-defined information packet upon the successful resolution of debugging the portion of the matched protocol-defined information packet ~~wherein the module which puts the information onto the interconnect which matches the one or more conditions is prevented by the preventing circuitry from being granted access to the interconnect~~.

8. (currently amended) A circuit as claimed in claim 1, wherein said debug module is on said interconnect ~~the determining circuitry comprises comparator circuitry which compares the information on the interconnect with one or more match conditions~~.

9. (Previously Presented) A circuit as claimed in claim 1, wherein said conditions comprise one or more preconditions and one or more match conditions, said circuitry for preventing a module from putting information onto said interconnect when said one or more preconditions and said one or more match conditions occur.

10. (Original) A circuit as claimed in claim 9, wherein one precondition is that the one or more match conditions have occurred a predetermined number of times.

11. (Original) A circuit as claimed in claim 9, wherein one precondition is that the circuit is enabled.

12. (Original) A circuit as claimed in claim 9, wherein one precondition is that circuitry external to said circuit has been enabled.

13. (Original) A circuit as claimed in claim 12, wherein said external circuitry is a latch.

14. (Original) A circuit as claimed in claim 9, wherein said match conditions comprise one or more of the following:

an address or address range of the information;

the module or modules which put the information onto the interconnect;

the module or modules which are intended to receive the information on the interconnect; and

the type of transaction to which the information relates.

15. (Previously Presented) A circuit as claimed in claim 1, wherein storing circuitry is provided to store the information which satisfies the one or more conditions.

16. (Currently Amended) A functional circuit comprising: an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring protocol-defined information packets put onto the interconnect for analysis by one or more modules, said protocol-defined information packets being either a response protocol-defined information packet or a request protocol-defined information packet, and wherein both types of protocol-defined information packets include ~~including both~~ data, transaction type and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data and said monitoring circuit comprising:

circuitry for determining [[if]]whether at least a portion of the protocol-defined information packet on the interconnect matches one or more conditions and for identifying a source of the matched portion of the protocol-defined information packet; [[and]]

circuitry for preventing ~~a module~~ the source of the matched portion of the protocol-defined information packet from putting further information onto said interconnect [[if]]when it is determined that the protocol-defined information packet on the interconnect matches said one or more conditions; and

circuitry for communicating the portion of the matched protocol-defined information packet to a debug module on the interconnect for debugging.

17. (Currently Amended) A circuit as claimed in claim 16, wherein the request protocol-defined information packet includes an op-code field defining size and type of transaction. ~~circuit is an integrated circuit.~~

18. (currently amended) A circuit as claimed in claim 16, further comprising circuitry for arbitrating access to said interconnect between said modules so as to allow more than one request or response packets to be placed on the interconnect at the same time ~~wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time, said arbiter being connected to the preventing circuitry, the arbiter and the preventing circuitry being arranged so that a module which is prevented from putting further information onto the interconnect is prevented from winning an arbitration~~.

19. (Currently amended) A circuit as claimed in claim [[18]]16, wherein said determining circuitry is at least partially in the arbitrating circuitry ~~arbiter~~.

20. (Currently amended) A circuit as claimed in claim 16, wherein said interconnect is a split transaction bus.

21. (Currently Amended) A circuit as claimed in claim 16, further comprising circuitry to capture the matched portion of the protocol-defined information packet for further analysis ~~wherein one of said modules comprises a debug module~~.

22. (Currently Amended) A circuit as claimed in claim [[16]]21, wherein said ~~preventing~~ arbitrating circuit is in said debug module.

23. (Original) A circuit as claimed in claim 22, wherein at least part of the determining circuitry is in the debug module.

24. (Currently Amended) A circuit comprising:

an interconnect;

one or more modules connected to the interconnect to put protocol-defined information packets onto the interconnect for analysis, wherein the protocol-defined information packets are either a response protocol-defined information packet or a request protocol-defined information packet, and wherein both types of protocol-defined information packets include ~~comprise both~~ data, transaction type and packet routing information, said request protocol-defined information packet further including size information, and wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

an arbiter for determining which module is permitted to put protocol-defined information packets onto the interconnect; and

circuitry for preventing a module from putting further protocol-defined information packets onto said interconnect, said preventing circuitry preventing a module from winning an arbitration carried out by said arbiter.

25. (Currently Amended) A method comprising the steps of:

monitoring protocol-defined information packets on an interconnect, the information comprising data and packet routing information and being put onto the interconnect by one or modules for analysis including circuit debugging, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

determining [[if]]whether the information on an interconnect satisfies one or more conditions and responsive to determining that the information satisfies one or more conditions identifying a source of the information; [[[and]]

preventing a the source of the information determined to satisfy one or more conditions ~~module~~ from putting additional protocol-defined information packets onto an interconnect ~~if it is determined that the information satisfies one or more conditions~~; and

arbitrating access to said interconnect between said modules allowing one or more of the request or response packets to be placed on the interconnect at the same time.

26. (Currently Amended) A circuit for monitoring protocol-defined packet information put onto an interconnect by one or more modules for analysis including debugging of the circuit, wherein said interconnect is not a circuit-switched bus, wherein each protocol-defined packet comprises a number of fields containing information, including a routing field, an address field, a source field, a transaction type field, a transaction size field, a transaction identifier field, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules, said circuit comprising:

circuitry for determining [[if]]whether the information in a protocol-defined packet matches one or more conditions; and

circuitry for preventing a module from putting further protocol-defined information packets onto said interconnect [[if]]when it is determined that information on the interconnect matches said one or more conditions and arbitrating between said modules for access to said interconnect allowing one or more of the request or response packets to be placed on the interconnect at the same time.